IN THE CLAIMS:

Kindly amend the claims, as follows:

1. (Previously Presented) A signal processing apparatus comprising:

an input circuit to receive an input signal;

a high-pass filter responsive to said input circuit,

wherein said high-pass filter comprises M taps to filter precursor intersymbol interference (ISI), one main tap and N taps to filter postcursor ISI, and

wherein adaptation of each of said N taps is limited to a range of between -1 and 0; and

a decision feedback equalizer comprising:

a decision circuit responsive to said high-pass filter; and

a feedback filter responsive to said decision circuit,

wherein said decision circuit is responsive to said feedback filter.

2. (Previously Presented) A signal processing apparatus according to Claim 1, wherein said high-pass filter has a low cutoff' frequency.

3. (Previously Presented) A signal processing apparatus according to Claim 2, wherein said high-pass filter has a flat response.

4. (Previously Presented) A signal processing apparatus according to Claim 1, wherein said high-pass filter has high attenuation at low frequency.

5. (Previously Presented) A signal processing apparatus according to Claim 1, wherein said high-pass filter has high attenuation at low frequencies.

6. (Previously Presented) A signal processing apparatus according to Claim 5, wherein the high attenuation is at least 20 db.

7. (Canceled)

8. (Previously Presented) A signal processing apparatus, comprising:

an input circuit to receive an input signal;

a feedforward equalizer comprising a high-pass filter and responsive to said input circuit,

wherein said high-pass filter comprises a finite impulse response (FIR) filter,

wherein said FIR filter comprises M taps to filter precursor intersymbol interference (ISI), one main tap and N taps to filter postcursor ISI, and

wherein adaptation of each of said N taps is limited to a range of between -1 and 0;

a decision feedback equalizer comprising:

a decision circuit responsive to said feedforward equalizer; and

a feedback filter responsive to said decision circuit,

wherein said decision circuit is responsive to said feedback filter.

9. (Currently Amended) A signal processing apparatus, comprising:

an input circuit to receive an input signal;

a feedforward equalizer comprising a high-pass filter and responsive to said input circuit,

wherein said high-pass filter comprises a finite impulse response (FIR) filter,

wherein said FIR filter comprises M taps to filter precursor intersymbol interference (ISI), one main tap and N taps to filter postcursor ISI,

wherein each tap of said FIR filter has a corresponding coefficient W as follows:

$$W_0 = \text{unity}$$

$$0 < \sum_{1}^{M} W_{-i} + W_o + \sum_{1}^{n} W_i << 1, \text{ and}$$

$$-1 \text{ [[<<]]} \leq W_1, \ldots W_n \text{ [[<<]]} \leq 0; \text{ and}$$

a decision feedback equalizer comprising:

a decision circuit responsive to said feedforward equalizer; and

a feedback filter responsive to said decision circuit,

wherein said decision circuit is responsive to said feedback filter.

10. (Previously Presented) A signal processing apparatus according to Claim 1, wherein said input circuit comprises an analog to digital converter.

11. (Previously Presented) A signal processing apparatus according to Claim 1, wherein said decision circuit comprises a threshold circuit.

12. (Previously Presented) A signal processing apparatus according to Claim 1, wherein said decision circuit comprises a Viterbi detector.

13. (Previously Presented) A signal processing apparatus, comprising:

an input circuit to receive an input signal;

a feedforward equalizer comprising a high-pass filter and responsive to said input circuit,

wherein said high-pass filter comprises a finite impulse response (FIR) filter, and

wherein said FIR filter comprises M taps to filter precursor intersymbol interference (ISI), one main tap and N taps to filter postcursor ISI;

an adaptive control circuit to adapt the M taps for filtering the precursor ISI and N taps for filtering the postcursor ISI; and

a decision feedback equalizer comprising:

a decision circuit responsive to said feedforward equalizer; and

a feedback filter responsive to said decision circuit,

wherein said decision circuit is responsive to said feedback filter.

14. (Previously Presented) A signal processing apparatus according to Claim 13,

wherein each of the N taps comprises a limiter to limit the range of adaptation of the N taps.

15. (Previously Presented) A signal processing apparatus according to Claim 13, wherein said adaptive control circuit is operable only during signal acquisition.

16. (Previously Presented) A signal processing apparatus according to Claim 1, wherein said feedback filter comprises a finite impulse response (FIR) filter.

17. (Previously Presented) A signal processing apparatus according to Claim 16, further comprising an adaptive control circuit to adapt taps of said FIR filter.

18. (Previously Presented) A signal processing apparatus comprising:

input means for receiving an input signal;

high-pass filtering means for filtering the input signal received by said input means,

wherein said high-pass filtering means comprises M taps to filter precursor intersymbol interference (ISI), one main tap and N taps to filter postcursor ISI, and

wherein adaptation of each of said N taps is limited to a range of between -1 and 0; and

decision feedback equalizer means comprising:

decision means responsive to said high-pass filtering means for recovering data from an output of said high-pass filtering means; and

feedback filter means for filtering an output of said decision means,

wherein said decision means is responsive to said feedback filter means.

19. (Previously Presented) A signal processing apparatus according to Claim 18, wherein said high-pass filtering means has a low cutoff frequency.

20. (Previously Presented) A signal processing apparatus according to Claim 19, wherein said high-pass filtering means has a flat response.

21. (Previously Presented) A signal processing apparatus according to Claim 18, wherein said high-pass filtering means has high attenuation at low frequency.

22. (Previously Presented) A signal processing apparatus according to Claim 18, wherein said high-pass filtering means has high attenuation at low frequencies.

23. (Previously Presented) A signal processing apparatus according to Claim 18, wherein said high-pass filtering means shortens a length of postcursor ISI.

24. (Previously Presented) A signal processing apparatus according to Claim 18, wherein said high-pass filtering means attenuates DC noise.

25. (Previously Presented) A signal processing apparatus according to Claim 18, wherein said high-pass filtering means attenuates baseline wander.

26. (Previously Presented) A signal processing apparatus according to Claim 22, wherein the high attenuation is at least 20 db.

27. (Canceled)

28. (Previously Presented) A signal processing apparatus comprising:

input means for receiving an input signal;

feedforward equalizer means for feedforward equalizing by high-pass filtering the input signal received by said input means,

wherein said feedforward equalizer means comprises a finite impulse response (FIR) filter means for filtering the input signal,

wherein said FIR filter means comprises M taps for filtering precursor intersymbol interference (ISI), one main tap and N taps for filtering postcursor ISI, and

wherein adaptation of each of said N taps is limited to a range of between -1

and 0; and

decision feedback equalizer means comprising:

decision means for recovering data from an output of said feedforward equalizer means; and

feedback filter means for filtering an output of said decision means,

wherein said decision means is responsive to said feedback filter means.

29. (Currently Amended) A signal processing apparatus, comprising:

input means for receiving an input signal;

feedforward equalizer means for feedforward equalizing by high-pass filtering the input signal received by said input means,

wherein said feedforward equalizer means comprises a finite impulse response (FIR) filter means for filtering the input signal,

wherein said FIR filter means comprises M taps for filtering precursor intersymbol interference (ISI), one main tap and N taps for filtering postcursor ISI,

wherein each tap of said FIR filter means has a corresponding coefficient W as follows:

W_0 = unity

$$0 < \sum_{1}^{M} W_{-i} + W_o + \sum_{1}^{n} W_i << 1, \text{ and}$$

-1 [[<<]] $\leq W_1, \ldots W_n$ [[<<]] ≤ 0; and

decision feedback equalizer means comprising:

decision means for recovering data from an output of said feedforward equalizer means; and

feedback filter means for filtering an output of said decision means,

wherein said decision means is responsive to said feedback filter means.

30. (Previously Presented) A signal processing apparatus according to Claim 18, wherein said input means comprises an analog to digital converter means for converting an analog input signal to a digital signal.

31. (Previously Presented) A signal processing apparatus according to Claim 18, wherein said decision means comprises a threshold circuit.

32. (Previously Presented) A signal processing apparatus according to Claim 18, wherein said decision means comprises a Viterbi detector.

33. (Previously Presented) A signal processing apparatus comprising:

input means for receiving an input signal;

feedforward equalizer means for feedforward equalizing by high-pass filtering the input signal received by said input means,

wherein said feedforward equalizer means comprises a finite impulse response (FIR) filter means for filtering the input signal, and

wherein said FIR filter means comprises M taps for filtering precursor intersymbol interference (ISI), one main tap and N taps for filtering postcursor ISI;

an adaptive control means for adapting the M taps for filtering the precursor ISI and N taps for filtering the postcursor ISI; and

decision feedback equalizer means comprising:

decision means for recovering data from an output of said feedforward equalizer means; and

feedback filter means for filtering an output of said decision means,

wherein said decision means is responsive to said feedback filter means.

34. (Previously Presented) A signal processing apparatus according to Claim 33, wherein each of the N taps comprises a limiting means for limiting the range of adaptation of the N taps.

35. (Previously Presented) A signal processing apparatus according to Claim 33, wherein said adaptive control means is operable only during signal acquisition.

36. (Previously Presented) A signal processing apparatus according to Claim 18, wherein said feedback filter means comprises a finite impulse response (FIR) filter means for filtering the output of said decision means.

37. (Previously Presented) A signal processing apparatus according to Claim 36, further comprising an adaptive control means for adapting taps of said FIR filter means.

38. (Previously Presented) An Ethernet transceiver, comprising:

an input circuit for inputting an input signal into an Ethernet cable;

an output circuit for outputting an output signal from the Ethernet cable, the output signal corresponding to the input signal;

a high-pass filter responsive to said input circuit,

wherein said high-pass filter comprises M taps to filter precursor intersymbol interference (ISI), one main tap and N taps to filter postcursor ISI, and

wherein adaptation of each of said N taps is limited to a range of between -1 and 0; and

a decision feedback equalizer comprising:

a decision circuit responsive to said high-pass filter; and

a feedback filter responsive to said decision circuit,

wherein said decision circuit is responsive to said feedback filter.

39. (Original) An Ethernet transceiver according to Claim 38, wherein said high-pass filter has a low cutoff frequency.

40. (Original) An Ethernet transceiver according to Claim 39, wherein said high-pass filter has a flat response.

41. (Original) An Ethernet transceiver according to Claim 38, wherein said high-pass filter has high attenuation at low frequency.

42. (Original) An Ethernet transceiver according to Claim 38, wherein said high-pass filter has high attenuation at low frequencies.

43. (Original) An Ethernet transceiver according to Claim 42, wherein the high attenuation is at least 20 db.

44. (Canceled)

45. (Previously Presented) An Ethernet transceiver, comprising:

an input circuit for inputting an input signal into an Ethernet cable;

an output circuit for outputting an output signal from the Ethernet cable, the output signal corresponding to the input signal;

a feedforward equalizer comprising a high-pass filter and responsive to said input circuit,

wherein said high-pass filter comprises a finite impulse response (FIR) filter,

wherein said FIR filter comprises M taps to filter precursor intersymbol interference (ISI), one main tap and N taps to filter postcursor ISI, and

wherein adaptation of each of said N taps is limited to a range of between -1 and 0; and

a decision feedback equalizer comprising:

a decision circuit responsive to said feedforward equalizer; and

a feedback filter responsive to said decision circuit,

wherein said decision circuit is responsive to said feedback filter.

46. (Currently Amended) An Ethernet transceiver, comprising:

an input circuit for inputting an input signal into an Ethernet cable;

an output circuit for outputting an output signal from the Ethernet cable, the output signal corresponding to the input signal;

a feedforward equalizer comprising a high-pass filter and responsive to said input circuit,

wherein said high-pass filter comprises a finite impulse response (FIR) filter,

wherein said FIR filter comprises M taps to filter precursor intersymbol interference (ISI), one main tap and N taps to filter postcursor ISI,

wherein each tap of said FIR filter has a corresponding coefficient W as follows:

W_0 = unity

$$0 < \sum_{1}^{M} W_{-i} + W_o + \sum_{1}^{n} W_i << 1, \text{ and}$$

-1 [[<<]] $\leq W_1, \ldots W_n$ [[<<]] ≤ 0; and

a decision feedback equalizer comprising:

a decision circuit responsive to said feedforward equalizer; and

a feedback filter responsive to said decision circuit,

wherein said decision circuit is responsive to said feedback filter.

47. (Original) An Ethernet transceiver according to Claim 38, wherein said input circuit comprises an analog to digital converter.

48. (Original) An Ethernet transceiver according to Claim 38, wherein said decision circuit comprises a threshold circuit.

49. (Original) An Ethernet transceiver according to Claim 38, wherein said decision circuit comprises a Viterbi detector.

50. (Previously Presented) An Ethernet transceiver, comprising:

an input circuit for inputting an input signal into an Ethernet cable;

an output circuit for outputting an output signal from the Ethernet cable, the output signal corresponding to the input signal;

a feedforward equalizer comprising a high-pass filter and responsive to said input circuit,

wherein said high-pass filter comprises a finite impulse response (FIR) filter,

and

wherein said FIR filter comprises M taps to filter precursor intersymbol interference (ISI), one main tap and N taps to filter postcursor ISI;

an adaptive control circuit to adapt the M taps for filtering the precursor ISI and N taps for filtering the postcursor ISI; and

a decision feedback equalizer comprising:

a decision circuit responsive to said feedforward equalizer; and

a feedback filter responsive to said decision circuit,

wherein said decision circuit is responsive to said feedback filter.

51. (Original) An Ethernet transceiver according to Claim 50, wherein each of the N taps comprises a limiter to limit the range of adaptation of the N taps.

52. (Previously Presented) An Ethernet transceiver according to Claim 50, wherein said adaptive control circuit is operable only during signal acquisition.

53. (Previously Presented) An Ethernet transceiver according to Claim 38, wherein said feedback filter comprises a finite impulse response (FIR) filter.

54. (Previously Presented) An Ethernet transceiver according to Claim 53, further comprising an adaptive control circuit to adapt taps of said FIR filter.

55. (Previously Presented) An Ethernet transceiver, comprising:

input means for receiving an input signal;

high-pass filtering means for filtering the input signal received by said input means,

wherein said high-pass filtering means comprises M taps to filter precursor intersymbol interference (ISI), one main tap and N taps to filter postcursor ISI, and

wherein adaptation of each of said N taps is limited to a range of between -1 and 0; and

decision feedback equalizer means comprising:

decision means responsive to said high-pass filtering means for recovering data from an output of said high-pass filtering means; and

feedback filter means for filtering an output of said decision means,

wherein said decision means is responsive to said feedback filter means.

56. (Previously Presented) An Ethernet transceiver according to Claim 55, wherein said high-pass filtering means has a low cutoff frequency.

57. (Previously Presented) An Ethernet transceiver according to Claim 56, wherein said high-pass filtering means has a flat response.

58. (Previously Presented) An Ethernet transceiver according to Claim 55, wherein said high-pass filtering means has high attenuation at low frequency.

59. (Previously Presented) An Ethernet transceiver according to Claim 55, wherein said high-pass filtering means has high attenuation at low frequencies.

60. (Previously Presented) An Ethernet transceiver according to Claim 55, wherein said high-pass filtering means shortens a length of postcursor ISI.

61. (Previously Presented) An Ethernet transceiver according to Claim 55, wherein said high-pass filtering means attenuates DC noise.

62. (Previously Presented) An Ethernet transceiver according to Claim 55, wherein said high-pass filtering means attenuates baseline wander.

63. (Original) An Ethernet transceiver according to Claim 59, wherein the high attenuation is at least 20 db.

64. (Canceled)

65. (Previously Presented) An Ethernet transceiver, comprising:

input means for receiving an input signal;

feedforward equalizer means for feedforward equalizing by high-pass filtering the input signal received by said input means,

wherein said feedforward equalizer means comprises a finite impulse response (FIR) filter means for filtering the input signal,

wherein said FIR filter means comprises M taps for filtering precursor intersymbol interference (ISI), one main tap and N taps for filtering postcursor ISI, and

wherein adaptation of each of said N taps is limited to a range of between -1 and 0; and

decision feedback equalizer means comprising:

decision means for recovering data from an output of said feedforward equalizer means; and

feedback filter means for filtering an output of said decision means,

wherein said decision means is responsive to said feedback filter means.

66. (Currently Amended) An Ethernet transceiver, comprising:

input means for receiving an input signal;

feedforward equalizer means for feedforward equalizing by high-pass filtering the input signal received by said input means,

wherein said feedforward equalizer means comprises a finite impulse response (FIR) filter means for filtering the input signal,

wherein said FIR filter means comprises M taps for filtering precursor intersymbol interference (ISI), one main tap and N taps for filtering postcursor ISI,

wherein each tap of said FIR filter means has a corresponding coefficient W as follows:

W_0 = unity

$$0 < \sum_{1}^{M} W_{-i} + W_o + \sum_{1}^{n} W_i << 1, \text{ and}$$

$$-1 \text{ [[<<]]} \leq W_1, \ldots W_n \text{ [[<<]]} \leq 0; \text{ and}$$

decision feedback equalizer means comprising:

decision means for recovering data from an output of said feedforward equalizer means; and

feedback filter means for filtering an output of said decision means,

wherein said decision means is responsive to said feedback filter means.

67. (Original) An Ethernet transceiver according to Claim 55, wherein said input means comprises an analog to digital converter means for converting an analog input signal to a digital signal.

68. (Original) An Ethernet transceiver according to Claim 55, wherein said decision means comprises a threshold circuit.

69. (Original) An Ethernet transceiver according to Claim 55, wherein said decision means comprises a Viterbi detector.

70. (Previously Presented) An Ethernet transceiver, comprising:

input means for receiving an input signal;

feedforward equalizer means for feedforward equalizing by high-pass filtering the input signal received by said input means,

wherein said feedforward equalizer means comprises a finite impulse response (FIR) filter means for filtering the input signal, and

wherein said FIR filter means comprises M taps for filtering precursor intersymbol interference (ISI), one main tap and N taps for filtering postcursor ISI;

an adaptive control means for adapting the M taps for filtering the precursor ISI and N taps for filtering the postcursor ISI; and

decision feedback equalizer means comprising:

decision means for recovering data from an output of said feedforward equalizer means; and

feedback filter means for filtering an output of said decision means,

wherein said decision means is responsive to said feedback filter means.

71. (Previously Presented) An Ethernet transceiver according to Claim 70, wherein each of the N taps comprises a limiting means for limiting the range of adaptation of the N taps.

72. (Previously Presented) An Ethernet transceiver according to Claim 70, wherein said adaptive control means is operable only during signal acquisition.

73. (Previously Presented) An Ethernet transceiver according to Claim 55, wherein said feedback filter means comprises a finite impulse response (FIR) filter means for filtering the output of said decision means.

74. (Previously Presented) An Ethernet transceiver according to Claim 73, further comprising an adaptive control means for adapting taps of said FIR filter means.